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Modeling of a EEPROM device based on silicon quantum dots embedded in high-k dielectrics

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Abstract

The write/erase (W/E) and data retention characteristics of a memory device based on silicon/oxide/silicon dot/oxide/silicon structure were simulated. It was demonstrated that the replacement of the top blocking SiO₂ with high-k dielectric results in several important improvements of memory characteristics. In particular, the application of high-k dielectric as a top oxide enhances the electric field in the tunnel oxide, which allows using a thicker bottom oxide to improve the data retention time. In addition, in a new device the magnitude of the W/E pulse and the programming time can also be reduced. A typical design of the new structure leads to a programming duration of 10 ms and maintains a memory window of 3 V after 10-year data retention.

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1. Introduction

Nowadays, the market share of Flash EEPROM has been comparable to those DRAM and microprocessor ones [1]. Several advanced structures of Flash EEPROM have been

developed. Most of them are either based on polycrystalline silicon floating gate [2] or silicon nitride silicon–oxide–nitride–oxide–silicon (SONOS) structures [3,4]. For a terabit memory array, it is necessary to use a 30–40 nm channel length. In principle, a SONOS structure can overcome this limitation, whereas the floating gate Flash device will encounter greater problems in this way, mainly because the charge in the floating gate

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structure can easily escape through the oxide pores [5] due to the high lateral conductivity in the floating gate. Therefore, in floating gate Flash devices the thick bottom oxide and usually hot carriers injections are used.

The lateral conductivity and, consequently, the leakage current can be suppressed in EEPROM structures based on isolated semiconductor dots embedded in dielectric. This kind of EEPROMs has been proposed recently [6–12]. In these devices, SiO₂ or Si₃N₄ were used as bottom tunnel dielectrics and SiO₂ was used as the top blocking oxide [6–11]. However, our opinion is that the proposed devices have one important disadvantage. Since the dielectric constant of SiO₂ is low ($\epsilon = 3.9$), the considerable part of electric potential drops on the top oxide and, consequently, the large electric field induces a significant parasitic current from the poly-Si gate. This effect should decrease the memory window.

Here, we propose to replace the SiO₂ top dielectric by some high-k materials. The most promising high-k dielectrics are ZrO₂, HfO₂ (dielectric constant $\epsilon \approx 25$), Y₂O₃ ($\epsilon \approx 15$), Al₂O₃ ($\epsilon \approx 10$) [13–15]. As it has already been shown the application of high-k dielectric as a blocking dielectric in the SONOS EEPROM would have several advantages, namely: the parasitic injection from the poly-Si gate can be suppressed, the write/erase (W/E) programming time and the voltage magnitude can be decreased [16–19]. In this paper, we present the results of a numerical simulation of W/E processes and retention characteristics of EEPROM based on silicon dots (SD) with SiO₂ and ZrO₂ top oxides.

2. Theoretical model

The proposed memory device with Si dots is shown in Fig. 1. One can see that the distances between SDs are comparable to their size. Therefore, the geometry is essentially three-dimensional. Nevertheless, for simplification of the simulation, we consider a one-dimensional vertical cross-section through one of the dots (see Fig. 1). Energy diagrams for this slice in the case of Si/SiO₂/SD/SiO₂/poly-Si and Si/SiO₂/SD/ZrO₂/poly-Si structures are shown in Fig. 2.

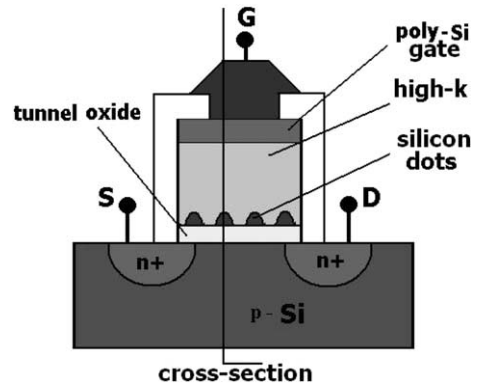


Fig. 1. Scheme of memory device based on Si dots embedded in high-k dielectric.

The electron and hole barriers at the Si/SiO₂ interface are 3.14 and 3.8 eV, respectively [20,21]. For the Si/ZrO₂ interface, several different values of electron barriers have been reported: 1.95 ± 0.08 eV [22], 2.0 eV [23] and 1.23 eV [24], although, the values of ZrO₂ bandgap in these studies are quite close 5.4 eV [23] and 5.5 eV [24]. In this work, the values used for the energy gap, electron and hole barriers at the Si/ZrO₂ interface are 5.5, 2.0 and 2.4 eV, respectively. Acceptor concentrations of the substrate and gate were 2×10^{14} cm⁻³ and the size of SD was 5.0 nm. The duration of W/E pulses in all cases was 10 ms. The thickness of the SiO₂ and top ZrO₂ tunnel oxides was 5.0 and 8.0 nm, respectively. One-dimensional and two-band model of charge transport was used. The Fowler–Nordheim (FN) model was adopted for the carrier injection from silicon substrate and poly-Si gate. For $F_{ox} \cdot d_{ox} > \Phi$ (where F_{ox} is electric field in oxide, d_{ox} is oxide thickness) the injection through the triangular barrier is described by

$$j = qnv \exp \left\{ -\frac{4}{3} \frac{\sqrt{2m^*}}{\hbar e} \frac{\Phi^{3/2}}{F_{ox}} \right\}, \quad (1)$$

where n is the carriers (hole or electron) density, v is their average velocity near Si/dielectric interface, and Φ is the Si/dielectric barrier. In the case of the trapezoidal barrier ($F_{ox} \cdot d_{ox} < \Phi$), the current injection is calculated by

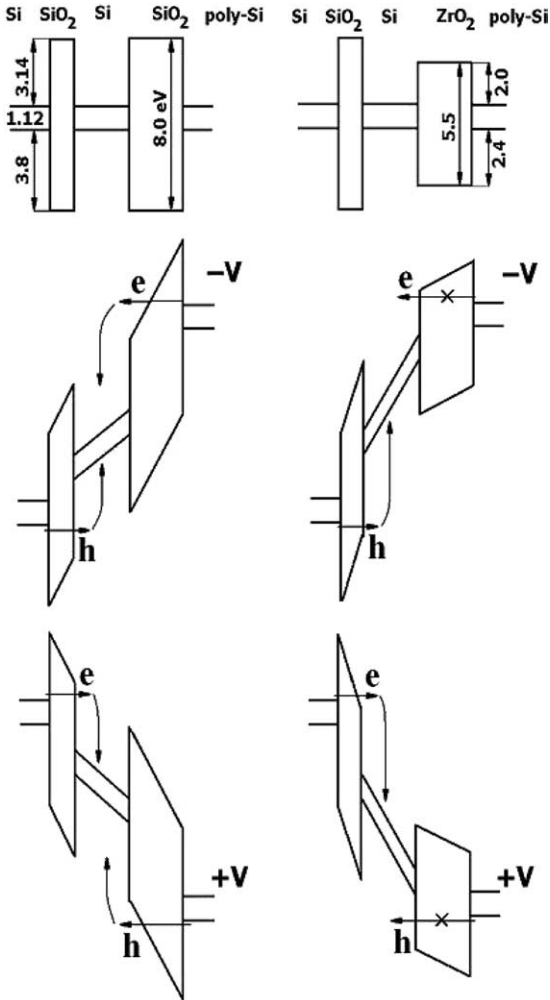


Fig. 2. Energy diagrams of Si/SiO₂/SD/SiO₂/poly-Si (left) and Si/SiO₂/SD/ZrO₂/poly-Si (right) structures under different biases: without bias (top), negative bias (middle); and positive bias (bottom). Band-bending is not shown for simplicity.

$$j = qnv \times \exp \left\{ -\frac{4}{3} \frac{\sqrt{2m^*}}{\hbar e} \frac{(\Phi^{3/2} - (\Phi - F_{ox}d_{ox})^{3/2})}{F_{ox}} \right\}. \quad (2)$$

This carrier density n is calculated from the voltage drop in semiconductor in self-consistent manner using the Fermi statistics for electrons and holes in semiconductor. To find the field distribution in the memory device, we have solved the Poisson equation for the given charge value in SD. The

escape current from SD has been calculated by the same Eqs. (1) and (2) but with the carrier density inside SD. Also, we have taken into account the quantum size effect, which reduces inner barrier heights for SD by the value

$$\Delta\Phi = \frac{3\pi^2\hbar^2}{2m^*L^2} \approx 0.15 \text{ eV},$$

where $L = 5 \text{ nm}$ is the dot size. This value is much less than barrier height 3.14 eV for electron on Si/oxide interface, therefore, this quantum effect does not significantly influence in simulation results of programming and retention modes.

The calculated memory parameter is the flat band voltage shift (U_{fb}) which is close to the threshold voltage (U_{th}) of the MOS transistor. For the retention mode simulation, we have used the same code with the zero applied voltage.

3. Results and discussion

At first we have simulated the W/E processes in the Si/SiO₂/SD/SiO₂/poly-Si structure with the bottom oxide of 1.5 nm thickness. As shown in Fig. 3 at the write pulse of +11 V, the flat band voltage is shifted up to +4 V due to electron injection into SD from substrate semiconductor. The erase pulse of -11 V shifts the flat band voltage to -2 V due to the holes accumulation in SD, so that the

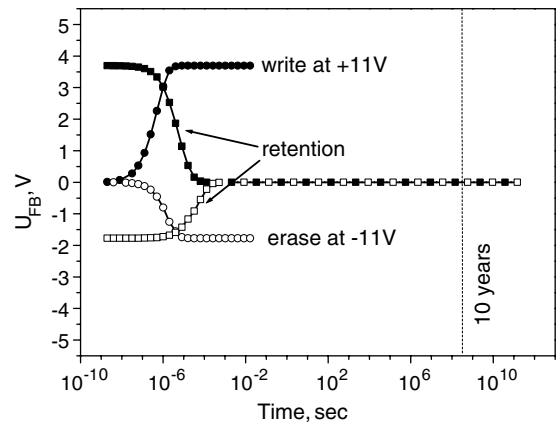


Fig. 3. Write/erase ($\pm 11 \text{ V}$) characteristics of Si/SiO₂/SD/SiO₂/poly-Si structure. Retention mode simulation was made for initial states after W/E pulses of 10 ms duration. The thickness of the top and bottom oxides are 5.0 and 1.5 nm, respectively.

memory window is 6 V. For the erase pulse, we have observed the electron parasitic injection through the blocking oxide. Unfortunately, the retention time is very short for this case 10^{-5} s, because of a charge stored in SD fast tunnels back into substrate through the relatively thin bottom oxide. So it is clear that to increase the retention time one needs to use a thicker bottom oxide. However, the application of the thicker bottom oxide drastically reduces the W/E memory window. For example, for the bottom oxide of 2.5 nm thickness, the memory window is less than 1 V and shifts to the positive domain (see Fig. 4). For this case, the hole injection current in the erase mode becomes less than the parasitic electron current through the top oxide and no positive charge accumulation in SD is observed. Even for 2.5 nm bottom oxide thickness the retention time is short ≈ 10 s.

For the thicker bottom oxide, both tunnel barriers of top and bottom oxides are triangle and the device becomes symmetric in the sense of the FN injection for both polarities of the applied bias. As a result the memory window vanishes. Thus, it is clear that the applying the same material as top and bottom oxides could not provide the required memory window and the 10 years retention time of the memory device based on SD. Therefore, we propose to replace the top SiO_2 ($\epsilon = 3.9$) oxide by high-k dielectric in particular ZrO_2 ($\epsilon = 25$). In this case, for the same device geometry

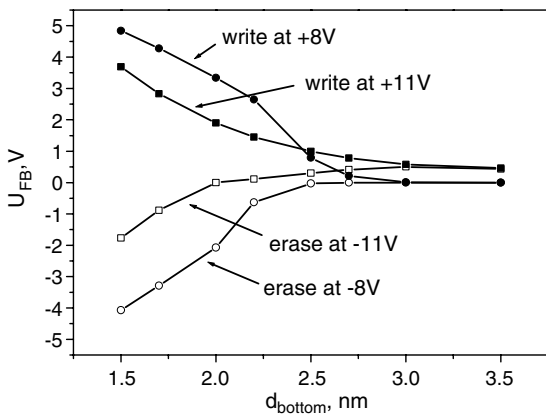


Fig. 4. Memory window for Si/SiO₂/SD/SiO₂/poly-Si structure as a function of bottom oxide thickness. The top oxide thickness is 5.0 nm and the W/E pulses are ± 11 or ± 8 V, pulse duration 10 ms.

and the fixed bias, the voltage drop in the top oxide decreases due to the large dielectric constant of ZrO_2 , while the one in bottom oxide increases. The last means an enhancement of the electric field in the bottom oxide. Energetic diagrams for both polarities reported in Fig. 2 illustrate this effect. The effect of field enhancement allows to use a thicker bottom oxide keeping the same time of write or erase processes.

As it is shown in Fig. 5, the memory window is about of 3 V for the structure with 5.0 nm SiO_2

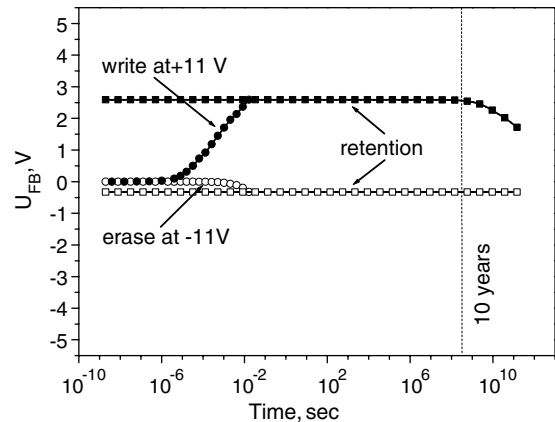


Fig. 5. Write/erase characteristics for the Si/SiO₂/SD/ZrO₂/poly-Si structure. Retention mode simulation was made for initial states after W/E pulses of 10 ms duration. The thickness of top and bottom oxides are 8.0 and 5.0 nm, respectively.

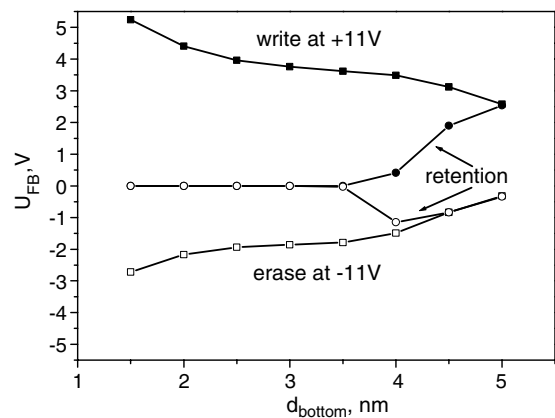


Fig. 6. Memory window for Si/SiO₂/SD/ZrO₂/poly-Si structure vs. bottom oxide thickness after W/E pulses of 10 ms duration. Also, the memory window after 10 years retention is shown. The thickness of top oxide is 8.0 nm.

bottom oxide thickness and ZrO_2 as a top oxide. For this case, we did not see a parasitic current from the gate due to FN tunneling because of the small electric field in the top oxide. The thick bottom oxide prevents the charge escape from SD and provides a good retention (see Fig. 5).

Fig. 6 demonstrates the simulated memory window vs. the bottom oxide thickness immediately after the W/E cycle and after 10 years. The noticeable memory window after 10 years can be obtained for a bottom oxide thicker than 3.5 nm.

4. Conclusion

By simulation we have shown that Si/SiO₂/SD/SiO₂/poly-Si structure can not provide a required sufficient large memory window and a good (10 years) retention simultaneously. The replacement of the top silicon oxide by a high-k ZrO_2 oxide increases the electric field in the bottom oxide and hence enhances the substrate current injection. This effect allows a thicker bottom oxide and improves the data retention time. In addition, a lower W/E voltage can be used and the programming time can be reduced at the same memory window. Since the voltage drop on the top oxide is reduced, the parasitic injection through the top oxide from the poly-Si gate can also be suppressed effectively. In the new structure, the data retention time of about 10 years can be achieved.

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