ISSN 8756-6990, Optoelectronics, Instrumentation and Data Processing, 2009, Vol. 45, No. 4, pp. 348–352. © Allerton Press, Inc., 2009.
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MATERIALS AND TECHNOLOGIES
FOR NANO- AND OPTOELECTRONICS

Optimization of the Dielectric Constant of a Blocking Dielectric in the Nonvolatile Memory Based on Silicon Nitride

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Received May 19, 2009

Abstract—It is shown that the blocking layer of the flash memory element based on silicon nitride has an optimal value of the dielectric constant, which allows the maximum memory window in the write/erase regime to be reached.

DOI: 10.3103/S8756699009040116

Key words: flash memory, blocking dielectric, silicon nitride.

INTRODUCTION

Flash devices with a floating gate are gradually replaced by devices based on silicon nitride as a storage medium: polySi–SiO_2–Si_3N_4–SiO_2–Si (SONOS) and metal–Al_2O_3–Si_3N_4–SiO_2–Si (MANOS) [1–3]. Pt or TaN (TANOS) is usually used as a metallic gate. In these devices, the information is stored in the form of a charge on electron and hole traps in silicon nitride. The blocking layer (BL) in TANOS structures is a dielectric with a high value of the dielectric constant (high-k dielectric), namely, Al_2O_3 ($\varepsilon = 10$) [1, 2]. Scaling (reduction of the memory cell size) requires the use of dielectrics with a higher value of the dielectric constant than that of Al_2O_3 as flash memory blocking layers. As was demonstrated in [4, 5], the use of high-k dielectrics [Al_2O_3, HfO_2, ZrO_2 ($\varepsilon = 25$)] instead of SiO_2 ($\varepsilon = 3.9$) usually used as a blocking layer allows one to reduce the programming time, decrease the programming voltage, reduce spurious injection, and increase the memory window (the difference between the flat-band voltages U_{FB} of the memory element in the logical states $\langle\langle 0 \rangle\rangle$ and $\langle\langle 1 \rangle\rangle$). On the other hand, high-k dielectrics allow using a thicker tunneling oxide, which is necessary for long-time storage of the charge in the memory cell (ten years at $T = 85°C$).

The objective of the present work was to demonstrate theoretically that there is an optimal value of the BL dielectric constant, such that deviations from this value deteriorate the performance of the flash memory structures based on silicon nitride (the calculations were performed for TANOS structures).

MODEL FOR CALCULATING THE WRITE/ERASE CHARACTERISTICS OF A TANOS STRUCTURE

Charge transport in Si_3N_4 is described by a bipolar model with the use of the one-dimensional Shockley–Read–Hall equation and the Poisson equation, which takes into account the nonuniform distribution of the electric field in silicon nitride [6, 7]. The injection currents through the tunneling and blocking oxides were calculated by the Fowler–Nordheim mechanism. Trap recharging was described by the multi-phonon ionization model. The parameters of the electron and hole traps in silicon nitride were assumed to be identical [6, 7], and their values were borrowed from [7]: optical energy $W_{opt} = 2.8$ eV, thermal energy $W_{th} = 1.4$ eV, phonon energy $W_{ph} = 60$ meV, effective mass $m^* = 0.5m_0$, capture cross section $\sigma = 5 \cdot 10^{-13}$ cm^2, and recombination cross section $\sigma^r = 5 \cdot 10^{-13}$ cm^2.

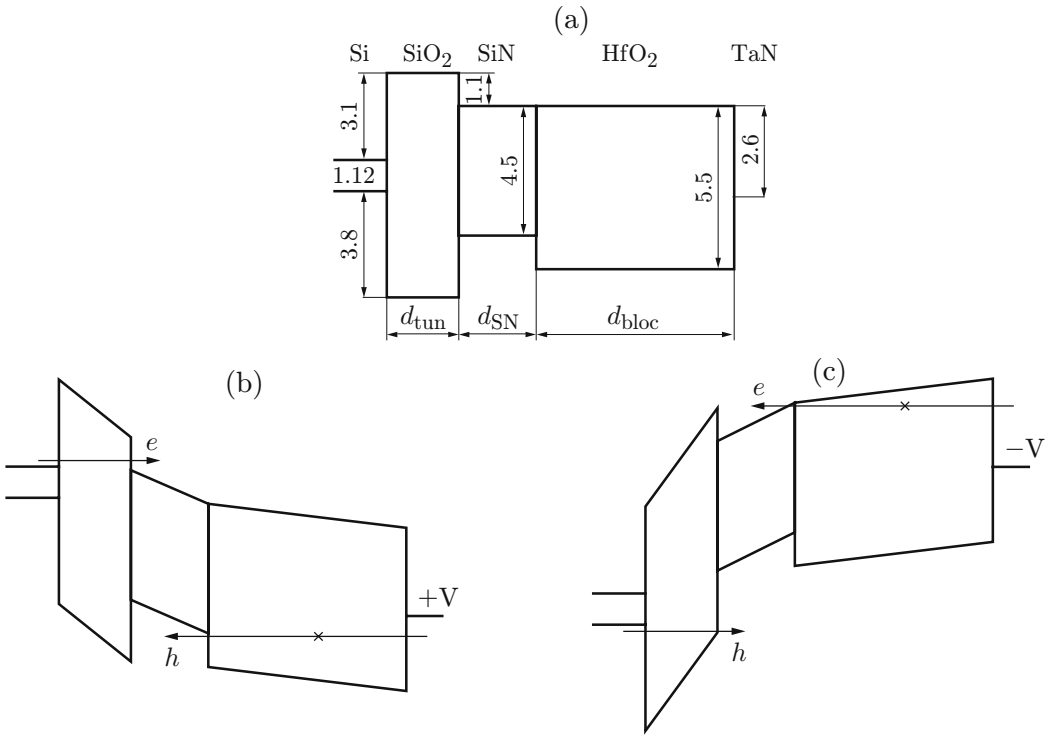

Fig. 1. Energy diagram of the TANOS structure: (a) without voltage applied; (b) with positive potential on the gate; (c) with negative potentials on the gate (the energy values are given in electron-volts).

The change in the flat-band voltage of the TANOS structure was calculated by the formula derived in [3]:

$$U_{\mathrm{FB}}(t) = \frac{q}{\varepsilon_0} \int\limits_0^{d_{\mathrm{SN}}} dx (n_t^e(x,t) - n_t^h(x,t)) \Big[\frac{d_{\mathrm{SN}} - x}{\varepsilon_{\mathrm{SN}}} + \frac{d_{\mathrm{bloc}}}{\varepsilon_{\mathrm{bloc}}} \Big]. \quad (1)$$

Here, $n_t^e(x)$ and $n_t^h(x)$ are the local concentrations of electrons and holes captures by traps in Si_3N_4, q is the electron charge, d_{SN} is the thickness of the silicon nitride layer, d_{bloc} is the BL thickness, ε_0 is the dielectric constant, and $\varepsilon_{\mathrm{SN}}$ and $\varepsilon_{\mathrm{bloc}}$ are the dielectric constants of silicon nitride and BL, respectively.

The energy diagram of the TANOS structure with different polarities of the applied voltage is shown in Fig. 1. The following values of thickness were used for this geometry: $d_{\mathrm{tun}} = 5$ nm (tunneling oxide), $d_{\mathrm{SN}} = 5$ nm (silicon nitride), and $d_{\mathrm{bloc}} = 15$ nm (blocking oxide). The duration of the write/erase pulse was 10 ms in all cases.

OPTIMIZATION OF THE BLOCKING DIELECTRIC

The write/erase characteristics calculated for a TANOS structure with three dielectrics (SiO_2, Al_2O_3, and HfO_2) used as the blocking layer, and also the memory window (MW) are shown in Fig. 2. The magnitude of the programming pulse $U_{w/e}$ was ±16 V, with a duration of 10 ms. The concentrations of electron and hole traps were assumed to be $N_t = 5 \cdot 10^{19}$ cm^{-3}. The estimates show that the smallest memory window is obtained if SiO_2 is used as the blocking dielectric. The reason is a significant drop of voltage of the writing (or erasing) pulse on the blocking layer. As a consequence, the voltage on the tunneling SiO_2 also decreases, which yields lower values of the Fowler–Nordheim injection current. Spurious injection is another typical feature of the TANOS structure with a SiO_2 blocking layer. The maximum memory window is obtained with the use of HfO_2 as the blocking layer. Because of the high value of the BL dielectric constant ($\varepsilon = 25$), the BL voltage drop becomes substantially smaller. At the same time, the voltage drop on the tunneling SiO_2 increases, which enhances the injection current through the SiO_2 tunneling layer in the write/erase regimes; hence, a larger memory window is obtained. Note that the value of the accumulated positive charge (erase mode) is smaller than the accumulated negative charge (write mode) because of the high energy barrier for holes at the Si/SiO_2 boundary (≈3.8 eV).

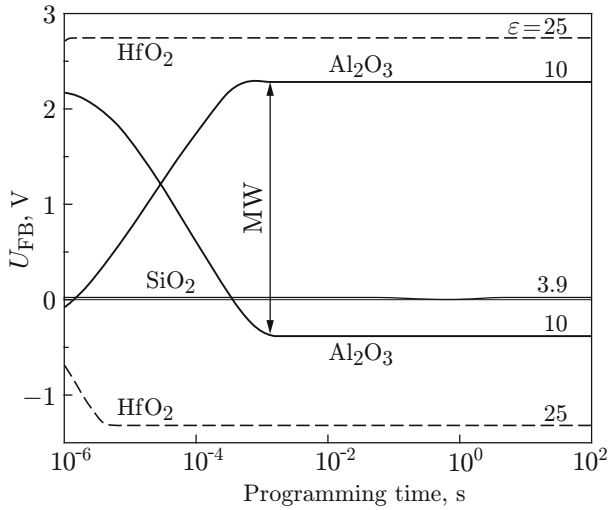

Fig. 2. Calculated write/erase characteristics of a TANOS structure for different dielectrics (SiO_2, Al_2O_3, and ZrO_2) used as the blocking layer.

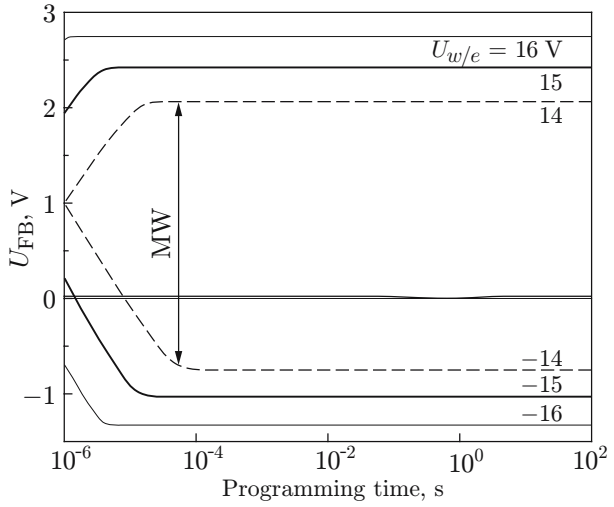

Fig. 3. Calculated write/erase characteristics of a TANOS structure for different voltages of pulses with a duration of 10 ms.

The calculated write/erase characteristics of the TANOS structure are plotted in Fig. 3 versus the magnitude of the writing (erasing) pulse. The amplitude of the programming pulse was $U_{w/e} = \pm 14$, ± 15, or ± 16 V. The HfO_2 high-k dielectric was used as the blocking dielectric. The concentrations of electron and hole traps were $N_t = 5 \cdot 10^{19}$ cm^{-3}. As the programming pulse amplitude is reduced from 16 to 14 V, the memory window decreases from 4.0 to 2.6 V, and the operation speed decreases approximately by two orders of magnitude.

The calculated dependences of the memory window size on the dielectric constant of the blocking oxide ($\varepsilon_{\text{bloc}}$) are shown in Fig. 4. The value $U_{w/e} = \pm 16$ V was used as the programming pulse amplitude. The concentrations of electron and hole traps were taken to be $N_t = 10^{19}$ (dashed curve) and $5 \cdot 10^{19}$ cm^{-3} (solid curve). The values of the electron energy barrier (2.6 eV) and hole energy barrier (2.9 eV) at the interface between TaN and high-k dielectric were used, as in the case with HfO_2. Note that minor deviations from these values of the energy barriers do not affect the TANOS structure performance, because there is practically no spurious injection if the high-k dielectric is used as the blocking layer. The calculations show that an increase in the dielectric constant of the blocking oxide ($\varepsilon_{\text{bloc}}$) ensures 1) a more intense electric

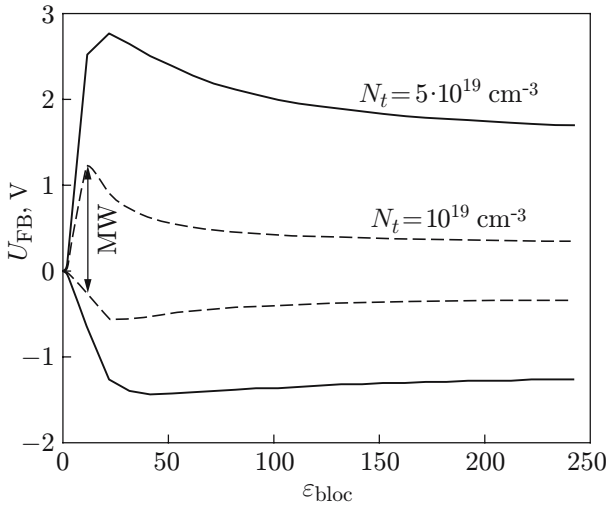

Fig. 4. Calculated memory window size versus the dielectric constant of the blocking oxide ($\varepsilon_{\text{bloc}}$) of a TANOS structure for different concentrations of electron and hole traps in Si_3N_4.

field in the tunneling oxide and a greater injection current in Si_3N_4, which favors an increase in the memory window size, and 2) a smaller voltage drop on the blocking oxide [see Eq. (1)], which favors a decrease in the memory window size.

The competition of these two processes yields the optimal value of the dielectric constant of the blocking dielectric ε = 20–30. A further increase in the dielectric constant does not affect the write/erase characteristics of the TANOS structure, because the voltage drop on the blocking layer tends to zero with increasing dielectric constant, and its contribution to flat-band voltage becomes negligibly small. Note that the maximum memory window of the TANOS structure for the trap concentration equal to $5 \cdot 10^{19}$ cm^{-3} is approximately twice greater than the maximum memory window for the trap concentration of 10^{19} cm^{-3} (see Fig. 4). It is known that enrichment of silicon nitride with silicon increases the total concentration of traps, whereas the depth of traps (thermal ionization energy) decreases [8]. For this reason, thicker layers of tunneling SiO_2 should be used to prevent charge drain from silicon-enriched silicon nitride to the silicon substrate. This is only possible by using high-k dielectrics as the blocking layer.

CONCLUSIONS

The effect of the dielectric constant of the blocking dielectric on the write/erase characteristics of a TANOS structure is considered. A typical feature of structures with low values of the dielectric constant of the blocking layer (smaller than 10) is a significant voltage drop on the blocking layer, leading to spurious injection, reduction of injection current through the tunneling oxide captured by charge traps, and constriction of the memory window. An increase in the dielectric constant of the blocking layer (to 10–25) leads to a smaller voltage drop on the blocking layer and, hence, to enhancement of the voltage drop on the tunneling oxide, which results in increasing injection current through the tunneling oxide captured by charge traps and in increasing the memory window size. A further increase in the dielectric constant of the blocking layer (above 25) leads to a decrease in the memory window owing to a smaller voltage drop on the blocking layer, which decreases almost to zero. The optimal value of the dielectric constant for the blocking oxide of the TANOS structure lies in the range of 20–30.

This work was supported by the Siberian Branch of the Russian Academy of Sciences (Integration Project No. 70) and by the Korean Ministry of Science and Technology (National Program for Tera-Level Nanodevice).

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